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Performance analysis of Optical Interleave Division Multiple Access using Turbo Encoder

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Abstract: The recent multiple access technique, known as interleave division multiple access with turbo encoder, is applied in wireless communication, as well as wired (optical) system to upgrade the performance of the system. The simulation has been done using MATLAB Simulink. The simulated results conforms that turbo encoder can be used to enhance the performance of OIDMA based wired (optical) system.

Keywords: ODMA scheme, Turbo encoder, BPSK modulation, Matrix interleavers, Turbo Decoder, Led, Photo diod.

1. INTRODUCTION

TURBO Coded OIDMA scheme is the next generation mobile communication systems i.e. 4th generation (4G) are needed to support multiple services in different types of environments [1-3]. 4G is being developed to accommodate the QoS (quality of service) and required data rate such as wireless broadband access, Multimedia Messaging Service (MMS), video chat, mobile TV. This paper recent multiple access techniques have been proposed with turbo encoder in 4G communication systems. [6]

The complete wireless communication system using IDMA scheme with turbo encoder has been shown in figure 1. The detail of IDMA system is shown in [1]. Here we replace the encoder with turbo encoder and analyse the performance of the system.

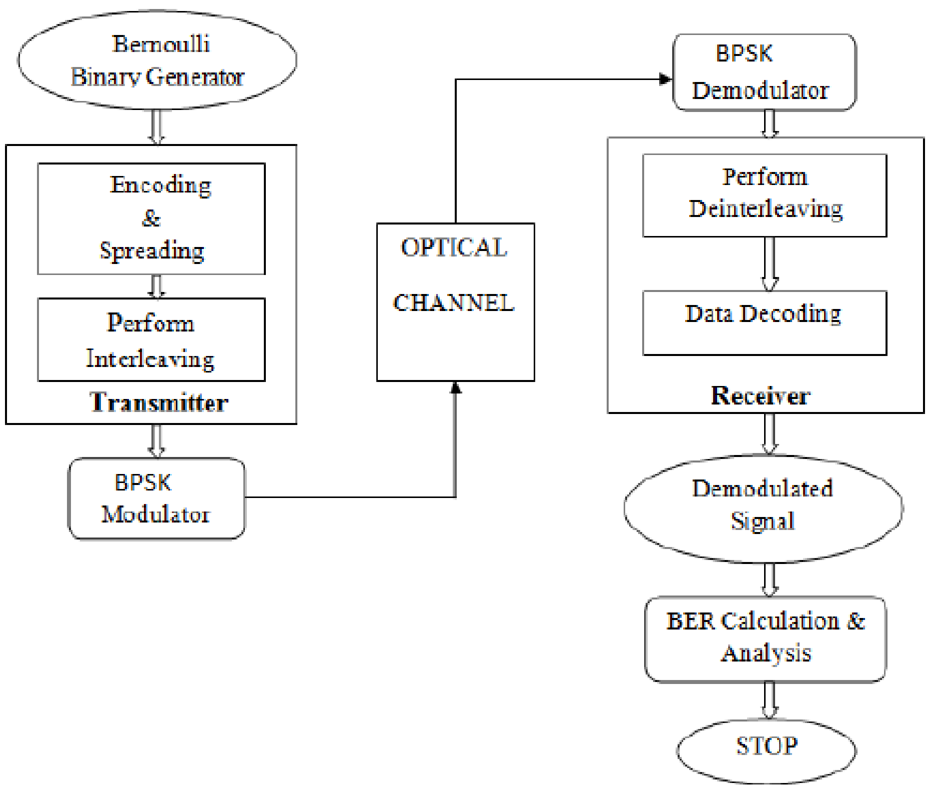

Figure 1: Transmitter and receiver configuration of turbo oidma system with k user.

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A communication system transmits information from one place to another, whether separated by a few kilometres or by transoceanic distances. Information is often carried by an electromagnetic carrier wave whose frequency can vary from a few mega-hertz to several hundred terahertzes. Optical communication systems use high carrier frequencies (~ 100 THz) in the visible or near-infrared region of the electromagnetic spectrum. They are sometimes called light wave systems to distinguish them from microwave systems, whose carrier frequency is typically smaller by five orders of magnitude (~1 GHz).

2. TURBO ENCODER

A Turbo encoder is a parallel concatenation scheme with multiple constituent Convolution encoders. The first encoder operates directly on the input bit sequence, while any others operate on interleaved input sequences, obtained by interleaving the input bits over a block length.

The internal pseudorandom inter leaver spread the data sequence. The System block based Turbo Encoder block uses two identical 8-state recursive systematic convolutional encoders. Figure 2 shows the basic configuration of turbo encoder, basically it is a recursive systematic encoder that employs two convolutional Encoders in parallel, where the second encoder is presented by an interleaver. The two recursive systematic convolutional encoder may be either identical or different. We observed that the nominal rate at the output at the turbo encoder is $R_{C=}1/3$. However by puncturing the parity check bits at the output of the binary convolutional encoder, we may achieve higher rate, such as rate 1/2 or 2/3. As in the case of concatenated block code, the Interleaver is usually selected to be a block pseudorandom interleaver that reorders the bits in the information sequence before feeding them to the second encoder. In effect, the use of two convolutional encoder in conjuction with the interleaver produces a code that contains very few code words of low weight .this characteristics does not necessarily imply that the free distance of the concatenated code is especially large, However, the use of the interleaver in conjunction with the two encoder result in code words that have relatively few nearest neighbors. That is, the code words are relatively sparse.

Hence the coding gain achieve by a turbo code is due in part to this feature, i.e. the reduction in the number of nearest neighboring code words that result from interleaving.

The second important aspect in achieving good performance with Turbo code is the use of iterative decoding based on the MAP criterion. The basic configuration of the iterative decoders Configuration shown in figure 3 and explanation has been presented in section 3.

We observed that the first decoder is provided with input from the demodulator corresponding to the information bits and the parity check bit P_1 .similarly the second decoder is provided with input from the demodulator corresponding to the Information bit and parity check bit $P_{2.}$

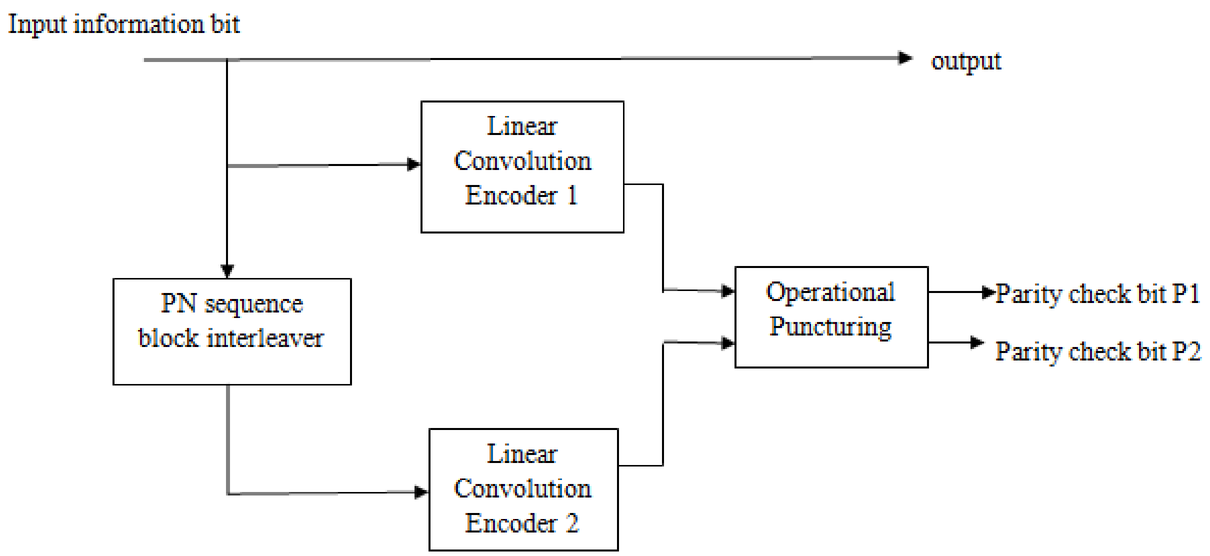

Figure 2: Internal structure of turbo encoder.

3. SIMULINK MODEL OF TRANSMITTER AND RECEIVER STRUCTURE OF IDMA SYSTEM WITH TURBO ENCODER

The Simulink model of the system is shown in figure 4 and consists all the blocks for simulation which is explain one by one.

Transmitter of Turbo coded oidma system: The transmitter of the turbo coded oidma system consist of Bernoulli binary generator, Turbo encoder, internal random interleaver, matrix interleaver, BPSK modulation, and AWGN channel. [4]

Bernoulli binary generator: This block generates a binary signal with a Bernoulli distribution.

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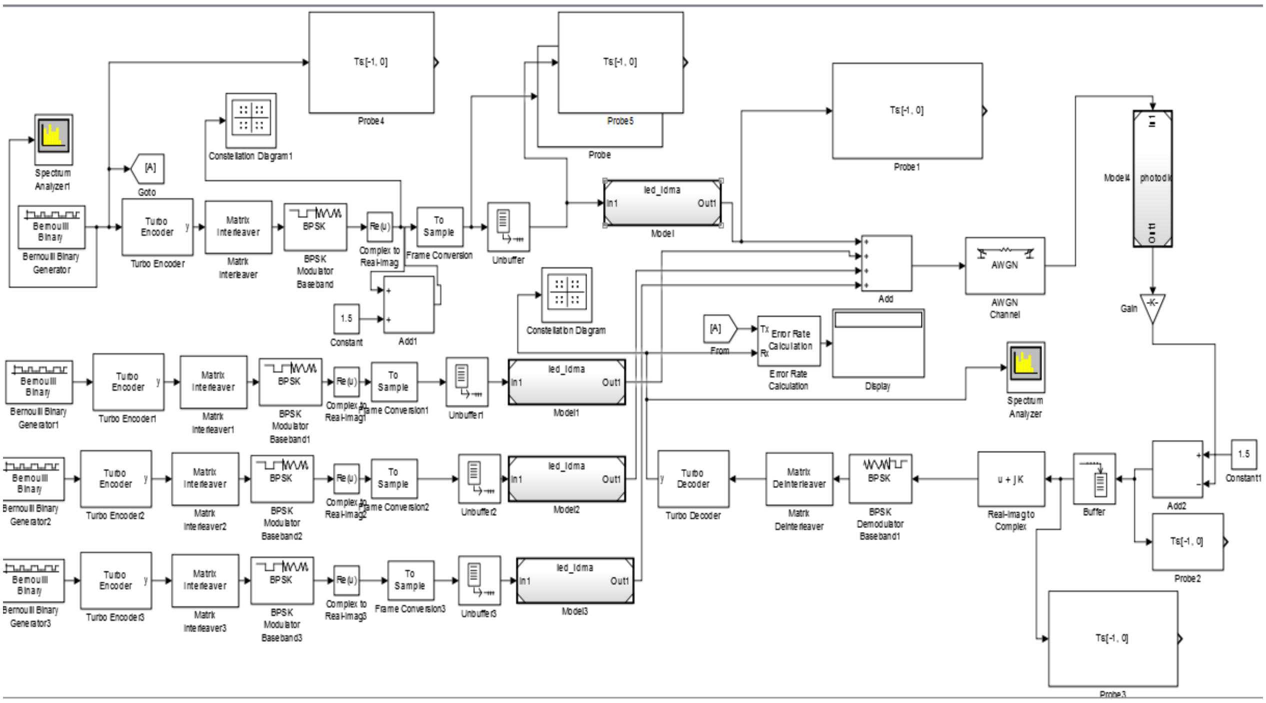

Figure 3: Simulink model of transmitter and receiver system oidma.

The model requires three main parameters to be set:
1. Probability of zeros
2. Seed
3. Sample time

In the simulation, probability of zeros is set to 0.5 means the same average number of ones and zeros occur in a particular time range. Seed defines the generator initial state and is set to 9876. The frame-based output with 180 samples per frame is to be set and output data type is set to be double.

Probe:
The Probe block outputs selected information about the signal on its input. The block can output the input signal's width, dimensionality, sample time, and a flag indicating whether the input is a complex-valued signal. The block has one input port. The number of output ports depends on the information that you select for probing, that is, signal dimensionality, sample time, and/or complex signal flag. Each probed value is output as a separate signal on a separate output port. The block accepts real or complex-valued signals of any built-in data type. It outputs signals of type double. During simulation, the block icon displays the probed data

Turbo Encoder: The turbo encoder is a forward error correcting code .That includes two recursive convolutional encoder and a pnsequence internal interleaver and punchring coder. The basic parameter of turbo encoder is Interleaver indices -:1:1.poly2trellis [4(13, 15)13]. Decoding algorithm True APP and chose decoding iteration. Typically, four iteration are Adequate if the decoders are operating at a high enough SNR to achieve an error rate in the range10^{-5} to10^{-6}, whereas, about eight to ten iteration may be needed when the error rate is in the Range of 10^{-5}, where the SNR is lower. [8]

Matrix Interleaver:Interleave the input vector by writing the elements into a matrix row-by-row and reading them out column-by-column. The product of Number of rows and Number of columns must match the input signal width. The matrix interleaver are converted total bit, in to row and coloum.

MODULATION OF OIDMA: The processes by which some characteristics of a carrier are varied by an information signal. Here we have use BPSK (Binary phase shift keying)/QPSK. BPSK provide 180 deg Phase shift. while QPSK provide 90 deg. Phase shift of carrier signal. This block accepts a column vector input signal. The input must be a discrete-time binary-valued signal. If the input bit is 0 or 1, respectively, then the modulated symbol is exp (jθ) or -exp (jθ), respectively, where θ represents the Phase offset parameter.

Real complex block
The Complex to Real-Imag block accepts a complex-valued signal of any data type that supports, including fixed-point data types. It outputs the real and/or imaginary part of the input signal, depending on the setting of the Output parameter. The real outputs are of the same data type as the complex input. The input can be an array (vector or matrix) of complex signals, in which case the output signals are arrays of the same dimensions. The real array contains the real parts of the corresponding complex input elements. The imaginary output similarly contains the imaginary parts of the input elements.

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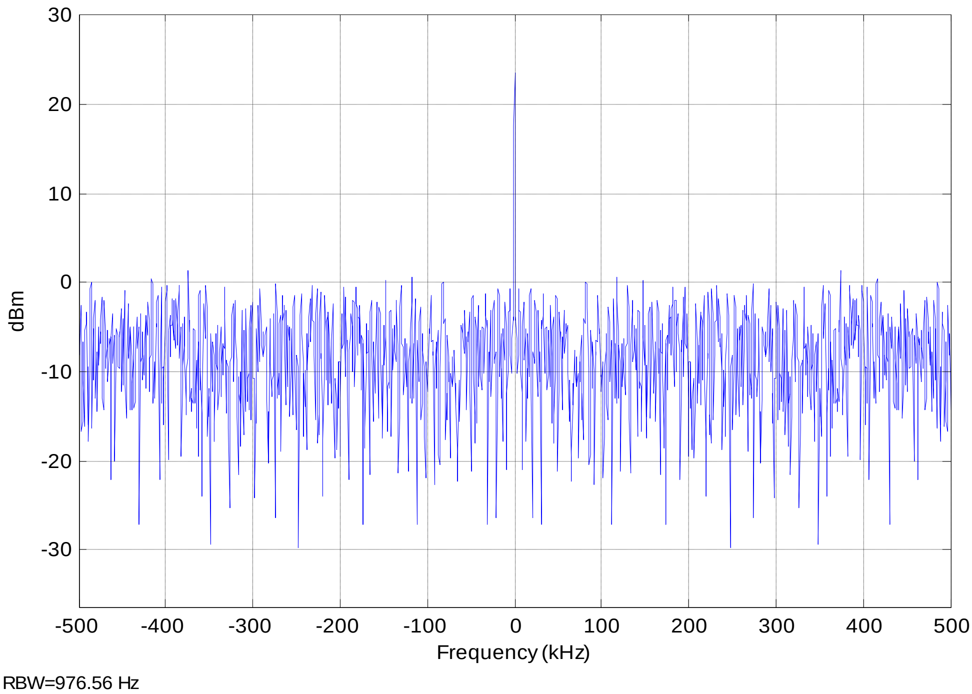

Fig4: Spectrum analyzer input

LED Block

The Light-Emitting Diode block represents a light-emitting diode as an exponential diode in series with a current sensor. The optical power presented at the signal port W is equal to the product of the current flowing through the diode and the Optical power per unit current parameter value. The exponential diode model provides the following relationship between the diode current I and the diode voltage V:

$$I = IS\left[e^{\frac{qV}{NkT_{m1}}} - 1\right]$$

where:

- q is the elementary charge on an electron (1.602176e–19 Coulombs).
- k is the Boltzmann constant (1.3806503e–23 J/K).
- N is the emission coefficient.
- IS is the saturation current.
- Tm1 is the temperature at which the diode parameters are specified, as defined by the Measurement temperature parameter value. When (qV / NkTm1) > 80, the block replaces with (qV / NkTm1 – 79)e80, which matches the gradient of the diode current at (qV / NkTm1) = 80 and extrapolates linearly. When (qV / NkTm1) < –79, the block replaces with (qV / NkTm1 + 80)e–79, which also matches the gradient and extrapolates linearly. Typical electrical circuits do not reach these extreme values. The block provides this linear extrapolation to help convergence when solving for the constraints during simulation. When you select Use parameters IS and N for the Parameterization parameter, you specify the diode in terms of the Saturation current IS and Emission coefficient N parameters. When you select Use I-V curve data points for the Parameterization parameter, you specify two voltage and current measurement points on the diode I-V curve and the block derives the IS and N values. When you specify current and voltage measurements, the block calculate IS and N as follows:

$$N = ((V_1 - V_2) / V_t) / (\log(I_1) - \log(I_2))$$

$$S = (I_1 / \exp(V_1 / (NV_t) - 1) + I_2(\exp(V_2/NV_t)) - 1))/2$$

where:

- $V_t = kT_{m1} / q$.
- V_1 and V_2 are the values in the Voltages $[V_1\ V_2]$ vector.
- I_1 and I_2 are the values in the Currents $[I_1\ I_2]$ vector.

The exponential diode model provides the option to include a junction capacitance:

When you select Fixed or zero junction capacitance for the Junction capacitance parameter, the capacitance is fixed. When you select Use parameters CJO, VJ, M & FC for the Junction capacitance parameter, the block uses the coefficients CJO, VJ, M, and FC to calculate a junction capacitance that depends on the junction voltage. When you select Use C-V curve data points for the Junction capacitance parameter, the block uses three capacitance values on the C-V capacitance curve to estimate CJO, VJ, and M and uses these values with the specified value of FC to calculate a junction capacitance that depends on the junction voltage. The block calculates CJO, VJ, and M as follows:

The reverse bias voltages (defined as positive values) should satisfy VR3 > VR2 > VR1. This means that the capacitances should satisfy C1 > C2 > C3 as reverse bias widens the depletion region and hence reduces

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capacitance. Violating these inequalities results in an error. Voltages VR2 and VR3 should be well away from the Junction potential VJ. Voltage VR1 should be less than the Junction potential VJ, with a typical value for VR1 being 0.1 V.The Light-Emitting Diode block contains several options for modeling the dependence of the diode current-voltage relationship on the temperature during simulation. Temperature dependence of the junction capacitance is not modeled, this being a much smaller effect.

The Light-Emitting Diode block has the following limitations:
When you select Use I-V curve data points for the Parameterization parameter, choose a pair of voltages near the diode turn-on voltage. Typically this is in the range from 0.05 to 1 Volt. Using values outside of this region may lead to numerical issues and poor estimates for IS and N. You may need to use nonzero ohmic resistance and junction capacitance values to prevent numerical simulation issues, but the simulation may run faster with these values set to zero.

AWGN Channel: The AWGN Channel block adds white Gaussian noise to a real or complex input signal. When the input signal is real, this block adds real Gaussian noise and produces a real output signal. When the input signal is complex, this block adds complex Gaussian noise and produces a complex output signal. This block accepts a scalar-valued, vector, or matrix input signal with a data type of type single or double. The output signal inherits port data types from the signals that drive the block. All values of power assume a nominal impedance of 1 ohm.[9]

Photo Diode Block:
The Photodiode block represents a photodiode as a controlled current source and an exponential diode connected in parallel. The controlled current source produces a current Ip that is proportional to the radiant flux density:

Ip = Device Sensitivity · Radiant Flux Density

Where:
Device Sensitivity is the ratio of the current produced to the incident radiant flux density. If you select Specify measured current forgiven flux density for the Sensitivity parameterization parameter, the block calculates this variable by converting the measured current parameter value to units of amps and dividing it by the Flux density parameter values.

If you select Specify current per unit flux density for the Sensitivity parameterization parameter, this variable is defined by the Device sensitivity parameter value. Radiant Flux Density is the incident radiant flux density. To model dynamic response time, use the Junction capacitance parameter to include the diode junction capacitance in the model. The exponential diode model provides the following relationship between the diode current I and the diode voltage V:

$$I = IS\left[e^{\frac{qV}{NkT_{m1}}} - 1\right]$$

where:

- q is the elementary charge on an electron (1.602176e–19 Coulombs).
- k is the Boltzmann constant (1.3806503e–23 J/K).
- N is the emission coefficient.
- IS is the saturation current, which is equal to the Dark current parameter value.
- Tm_1 is the temperature at which the diode parameters are specified, as defined by the Measurement temperature parameter value.

The Photodiode block has the following limitations: When you select Use dark current plus a forward bias I-V curve data point for the Diode parameterization parameter, choose a voltage near the diode turn-on voltage. Typically this will be in the range from 0.05 to 1 Volt. Using a value outside of this region may lead to a poor estimate for N. You may need to use nonzero ohmic resistance and junction capacitance values to prevent numerical simulation issues, but the simulation may run faster with these values set to zero.

Signal Processing and Input Dimensions: This block can process multichannel signals. When you set the Input Processing parameter to frame based, the block accepts an M-by-N input signal. M specifies the number of samples per channel and N specifies the number of channels. Both M and N can be equal to 1. The block adds frames of length-M Gaussian noise to each of the N channels, using a distinct random distribution per channel.

BPSK Demodulator: The BPSK Demodulator Baseband block demodulates a signal that was modulated using the binary phase shift keying method. The input is a baseband representation of the modulated signal.

This block accepts a scalar or column vector input signal. The input signal must be a discrete-time complex signal.

Matrix deinterleaver: Deinterleave the input vector by writing out row-by-row. The product of Number of rows and Number of columns must match the input signal width. The matrix deinterleaver convert Total bit in to, row and coloum.

TURBO DECODER: Decode input using a parallel concatenated decoding scheme that employs the a posteriori probability (APP) decoder as the constituent decoder. Both the constituent decoders use the same trellis structure and algorithm. Use the poly2trellis function to create a trellis using the constraint length, code generator (octal) and feedback connection (octal). Here we have use Interleaver indices -:1:1.polly2trellis [4(13, 15)13].Decoding algorithm True APP.[9]

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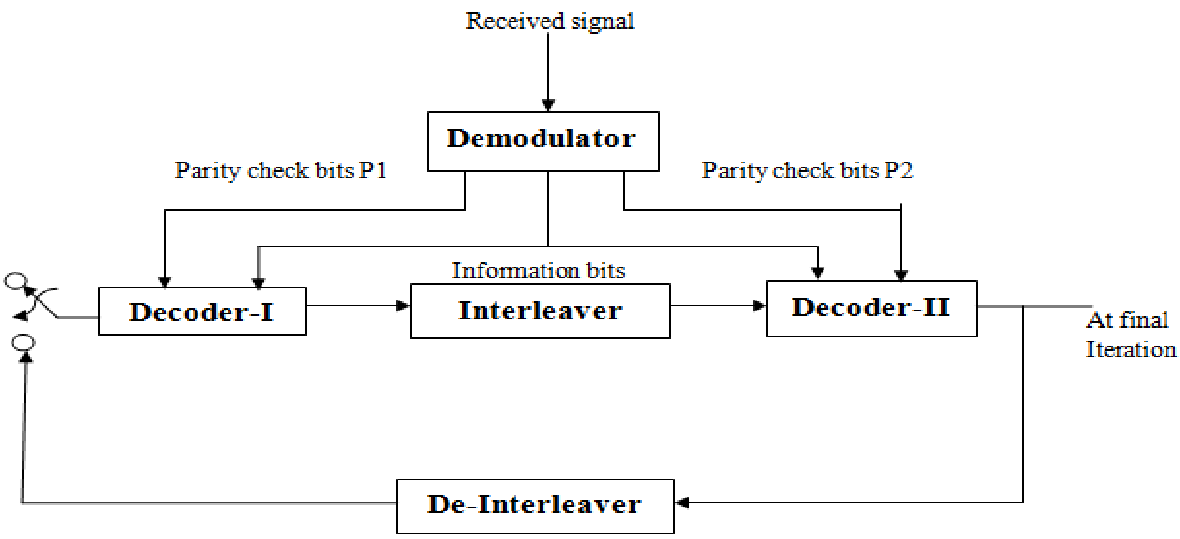

Figure 5: Turbo decoding

The Error Rate Calculation block

The Error Rate Calculation block compares input data from a transmitter with input data from a receiver. It calculates the error rate as a running statistic, by dividing the total number of unequal pairs of data elements by the total number of input data elements from one source. Use this block to compute either symbol or bit error rate, because it does not consider the magnitude of the difference between input data elements. If the inputs are bits, then the block computes.

4. RESULT AND DISCUSSION

The OIDMA system with Turbo encoder in wireless communication has been simulated and number of iteration is set to be 4 for optimum performance with minimum delay and complexity of the decoder are adequate if the decoders are operating at a high enough SNR to achieve an error rate in the range 10^{-5} to 10^{-6}, whereas, about eight to ten iteration may we needed when the error rate is in the range of 10^{-5}, where the SNR is lower. The future work of the turbo coded idma scheme is to reduce large interleavers decoding delay and the computational complexity inherent in the iterative decoding algorithm.

The output of the spectrum analyser is shown in figure (6). In X-axis show frequency in kHz and Y-axis show power in dBm.

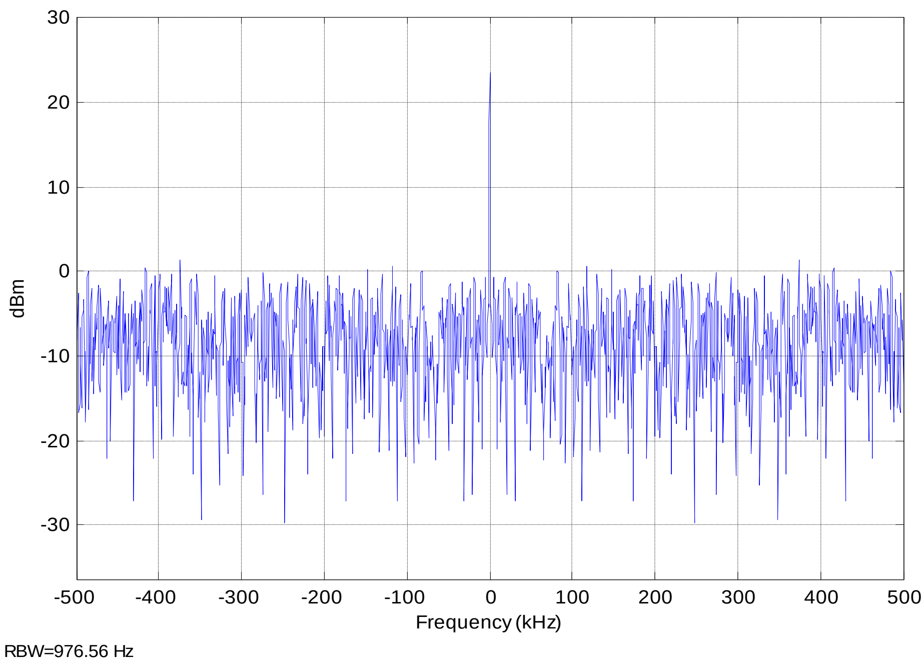

Fig6: Spectrum analyser output of oidma scheme with turbo encoder.

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The performance of OIDMA system has been compared with CDMA system and the results are shown in figure (7).

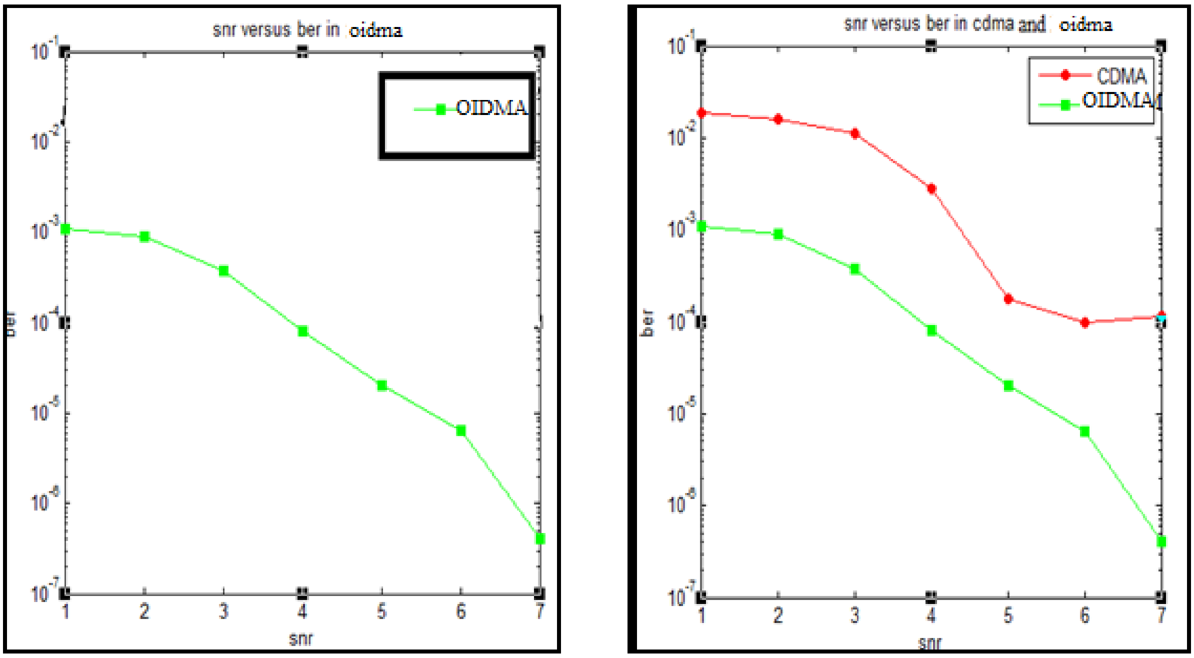

Fig7: Compare between CDMA systems Turbo coded OIDMA system .

5. CONCLUSION

In this paper, The Turbo coded OIDMA show high speed of communication services and low cost of receiver. Basically the Turbo code is high performance forward error correcting code it minimize the bit error rate on lower snr.The per-user computational complexity of the chip by chip is independent of the number of users involved. The Turbo coded oidma system provide Superior performance a rate ½ or 2/3 turbo code of block length $N=2^{12}$ with 4 iteration of decoding per bit, achieves an error probability of 10^{-5} at an SNR of 6 dB. The drawback of Iterative decoding is that it produces large decoding delay and computational complexity in the Iterative decoding algorithm. In most data communication system, however, the decoding delay is tolerable, and the additional computational complexity is usually justified by the significant Coding gain that is achieved by the turbo code. The OIDMA scheme with turbo encoder has been implemented in wireless communication using Simulink model of MATLAB software. The results confirm that the performance of the system can be improved with the use of turbo encoder.

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